CSC332  Fall 2018       HW3 (Paging)  
Due: Mon Nov 12  
  
Q1  
Consider the memory management scheme using paging. All numbers shown below and in your answer are in decimal.   
  
The page size is 16 bytes.  
  
The following table shows several logical addresses of process 5  
and their corresponding physical addresses:  
  
Logical address         Physical address  
---------------         ----------------  
  
53                              37  
  
17                              113  
  
35                              99  
  
9                               73  
  
55                              39  
  
Show the “page frame number” column in the first 4 rows (rows 0…3) of the page table of process 5.   
  
  
  
Q2.  
Consider a paging scheme.   
  
Suppose the page frame size is 64 bytes.  
  
Suppose all of process A is currently loaded in memory.  
  
Assume the page i of process A is loaded in page frame  
3i (for any page i of the process).  
  
In process A, there is an array B[0..100].  
Assume that each element of B occupies 4 bytes.  
  
The physical address of the beginning byte of B[50]   
(i.e., the byte 0 of B[50]) is 1390.  
  
Compute the physical address of B[100].  
  
Show your calculations. Clearly write down the final answer in one place.  
  
  
Q3.  
Consider memory management scheme using paging.   
  
Assume that the page size is 128 bytes. Assume that each logical address and physical address is 16 bits long.  
  
The entries in the page table for process 3, starting from row 0 of the table  
onwards, are: (Only the page frame number column is shown. These are shown in binary, spaces are included just for better readability):  
  
000 000 000   
100 111 010   
011 100 000   
000 010 000   
100 000 000   
101 000 000   
...  
...  
  
  
Convert the following PHYSICAL ADDRESSES  
to the corresponding LOGICAL ADDRESSES  
in process 3.   
These numbers are in BINARY,  
and your answer should also be in BINARY.  
  
Show details of your calculations.  
  
(a) 011 100 000 001 001 0  
(b) 101 000 000 010 010 1  
  
Q4.  
Consider the memory management scheme using paging.  
  
Let T be the page frame number column in the page table. Assume that the page table for process 2 satisfies T[i]=i+5 for all pages i.  
Assume that the page size is 256 bytes.  
  
Convert the following logical addresses in process 2 to   
the corresponding physical addresses. All numbers here and in your answer are in decimal.  
  
(a) 1021  
  
(b) 5933